CENTER FOR VLSI AND NANOTECHNOLOGY

Course Book for

M. Tech. in VLSI Design

For

Academic Year
2020 - 2021

Visvesvaraya National Institute of Technology,

Nagpur-440 010 (M.S.)

Institute Vision Statement

To contribute effectively to the National and International endeavour of producing quality human resource of world class standard by developing a sustainable technical education system to meet the changing technological needs of the Country and the World incorporating relevant social concerns and to build an environment to create and propagate innovative technologies for the economic development of the Nation.

Institute Mission Statement

The mission of VNIT is to achieve high standards of excellence in generating and propagating knowledge in engineering and allied disciplines. VNIT is committed to providing an education that combines rigorous academics with joy of discovery. The Institute encourages its community to engage in a dialogue with society to be able to effectively contribute for the betterment of humankind.

Department Vision Statement

The Department is committed to provide postgraduate academic and research programs to produce high quality human resource with ability to meet the global challenges in the field of VLSI Design and Nanoelectronics.

Department Mission Statement

The mission of the center is to achieve excellence in engineering education, research and professional service. It is endeavored to equip students to assume leadership positions in engineering practice, education, research and serve the mankind with most modern technology, serviceability and economy.

Brief about Center for VLSI and Nanotechnology:

The Center for VLSI and Nanotechnology started with the research facilities in the analog and digital domains and has grown steadfastly since its inception, expanding into the areas of nanoelectronics and MEMS. The center has excellent research facilities for carrying out research in different areas of Micro & Nano Electronics and VLSI. The center is actively involved in R & D as well as consultancy projects and has collaborations with several industries, academic institutes, and R&D organizations in the country. The laboratories are adequately equipped with state-of-the-art facilities.

List of faculty Members

Sr No	Faculty Name	Areas of specialization
1	Patrikar R. M.	VLSI, MEMS, Nanoelectronics
2	Deshmukh R. B.	VLSI Design, MEMS
3	Dhok S. B.	Digital Signal Processing, VLSI
4	Patil Ganesh C	Device Physics and Modeling, Novel Nanoscale MOSFETs, Analog/Digital CMOS circuits, VLSI System Design
5	Pulijala Vasu	RF Design, RF Magnetics, MEMS
6	Gupta Nikhil Deep	Opto-electronics, Photonics, Solar Cells, Nanotechnology, Renewable Energy, Nano-lithography processes
7	Deshmukh Sharvari	MEMS Sensors, Machine Olfaction, Machine Learning, Statistical Analysis

PG Programmes Offered by Center for VLSI and Nanotechnology:

The department offers following postgraduate programme

	Program	Description
PG	M. Tech. in VLSI Design	Intake 25

Credit System at VNIT :

Education at the Institute is organized around the semester-based credit system of study. The prominent features of the credit system are a process of continuous evaluation of a student's performance / progress and flexibility to allow a student to progress at an optimum pace suited to his/her ability or convenience, subject to fulfilling minimum requirements for continuation. A student's performance/progress is measured by the number of credits he/she has earned, i.e. completed satisfactorily. Based on the course credits and grades obtained by the student, grade point average is calculated. A minimum number of credits and a minimum grade point average must be acquired by a student in order to qualify for the degree.

Course credits assignment

Each course, except a few special courses, has certain number of credits assigned to it depending on lecture, tutorial and laboratory contact hours in a week.

For Lectures and Tutorials: One lecture hour per week per semester is assigned one credit and

For Practical/ Laboratory/ Studio: One hour per week per semester is assigned half credit.

Example: Course XXXXXX with (3-0-2) as (L-T-P) structure, i.e. 3 hr Lectures + 0 hr Tutorial + 2 hr Practical per week, will have (3x1 + 0x1 + 2x0.5 =) 4 credits.

Grading System

The grading reflects a student's own proficiency in the course. While relative standing of the student is clearly indicated by his/her grades, the process of awarding grades is based on fitting performance of the class to some statistical distribution. The course coordinator and associated faculty members for a course formulate appropriate procedure to award grades. These grades are reflective of the student's performance vis-à-vis instructor's expectation. If a student is declared pass in a subject, then he/she gets the credits associated with that subject.

Depending on marks scored in a subject, a student is given a Grade. Each grade has got certain grade points as follows:

Grade	Grade points	Description
AA	10	Outstanding
AB	9	Excellent
BB	8	Very good
BC	7	Good
CC	6	Average
CD	5	Below average
DD	4	Marginal (Pass Grade)
FF	0	Poor (Fail) /Unsatisfactory / Absence from end-sem exam
NP	-	Audit pass
NF	-	Audit fail
SS	-	Satisfactory performance in zero credit core course
ZZ	-	Unsatisfactory performance in zero credit core course
W	-	Insufficient attendance

Performance Evaluation

The performance of a student is evaluated in terms of two indices, viz, the Semester Grade Point Average (SGPA) which is the Grade Point Average for a semester and Cumulative Grade Point Average (CGPA) which is the Grade Point Average for all the completed semesters at any point in time. CGPA is rounded up to second decimal.

The Earned Credits (ECR) are defined as the sum of course credits for courses in which students have been awarded grades between AA to DD. Grades obtained in the audit courses are not counted for computation of grade point average.

Earned Grade Points in a semester (EGP) = **Σ** (Course credits x Grade point) for courses in which AA- DD grade has been obtained

SGPA = EGP / Σ (Course credits) for courses registered in a semester in which AA- FF grades are awarded

CGPA= EGP / Σ(Course credits) for courses passed in all completed semesters in which AA- DD grades are awarded

Overall Credits Requirement for Award of Degree

SN	Category of Course	Symbol	Credit Requirement (Minimum)			
			B. Tech. (4-Year)	B. Arch. (5 Year)	M. Tech. (2 Year)	M. Sc. (2 Year)
	Program Core					
1	Basic Sciences (BS)	BS	18	04	-	-
2	Engineering Arts & Sciences (ES)	ES	20	18	-	-
3	Humanities	HU/ HM*	05	06	-	-
4	Departmental core	DC	79-82	168	33-39	54-57
	Program Elective					
3	Departmental Elective	DE	33-48	17-23	13-19	06-09
4	Humanities & Management	HM	0-6	0-3	-	-
5	Open Course	OC	0-6	0-3	-	-
Total requirement :BS + ES + DC+ DE + HM + OC =			**170**	**219**	**52**	**63**
Minimum Cumulative Grade Point Average required for the award of degree			**4.00**	**4.00**	**6.00**	**4.00**

Attendance Rules

1. All students must attend every class and 100% attendance is expected from the students. However, in consideration of the constraints/ unavoidable circumstances, the attendance can be relaxed by course coordinator only to the extent of not more than 25%. Every student must attend minimum of 75% of the classes actually held for that course.
2. A student with less than 75% attendance in a course during the semester, will be awarded W grade. Such a student will not be eligible to appear for the end semester and re-examination of that course. Even if such a student happens to appear for these examinations, then, answer books of such students will not be evaluated.
3. A student with W grade is not eligible to appear for end semester examination, reexamination & summer term.

Program Outcomes (Department Specific) for M.Tech in VLSI Design

a) To obtain sound knowledge in the theory, principles and applications of VLSI Circuits and Systems.

b) Apply knowledge of VLSI Design Methods in the design and development of VLSI Systems.

c) Configure recent EDA tools, apply test conditions, and deploy and manage them.

d) Perform experiments on different CAD tools either obtained from external parties or developed in house and analyze the experimental results.

e) Design and implement projects given their specifications, within performance and cost constraints.

f) Identify, formulate and solve VLSI System Design problems and understand the project management issues.

g) Ability to understand the performance needs of interdisciplinary scientific and engineering disciplines and design and develop techniques for achieving these.

h) Acquire and understand new knowledge, use them to develop electronic products, and understand the importance of lifelong learning.

i) Ability to extend the state of art in some of the areas of interest and create new knowledge.

j) Communicate effectively in oral, written and graphical form.

k) Understand and formulate research problems and explore the current research being done.

l) Extend the state of art and explore new problems and solution techniques.

Scheme for M. Tech. (VLSI Design)

I To be offered in Odd Semester

Sr. No.	Course Code	Course Title	Type DC/DE	Structure L-T-P	Credits	Pre-requisites
1	ENL 509	Advanced Device Physics	DC	3-0-2	4	
2	ENL 511	CMOS Digital VLSI Design	DC	3-0-2	4	
3	ENL 513	IC Design with HDL	DC	3-0-2	4	
4	ENL 517	Micro and Nano Fabrication Technologies	DC	3-0-2	4	
5	END 501	Project - Phase I	DC	0-0-6	3	25 Credits
6	ENL 507	Design for Testability Yield and Reliability	DE	3-0-0	3	
7	ENL 521	Real Time Signal Processing	DE	3-0-0	3	
8	ENL 547	Spintronics	DE	3-0-0	3	
9	ENL 523	Display Materials and Technologies	DE	3-0-0	3	
10	ENL 543	Nanophotonics	DE	3-0-0	3	
11	ENL 545	VLSI Signal Processing	DE	3-0-0	3	
12	CSL 524	Real Time Systems	DE	3-0-0	3	

II To be offered in Even Semester

Sr. No.	Course Code	Course Title	Type DC/DE	Structure L-T-P	Credits	Pre-requisites
1	ENL518	Analog IC Design	DC	3-0-2	4	
2	ENL 520	Nanoelectronics	DC	3-0-2	4	
3	END 502	Project Phase-II	DC	0-0-18	9	35 Credits+ Project Phase-I
4	ENL 504	VLSI System Design	DE	3-0-0	3	
5	ENL 542	CMOS RF Design	DE	3-0-0	3	
6	ENL 522	MEMS and NEMS	DE	3-0-0	3	
7	ENL 546	Embedded Systems	DE	3-0-0	3	
8	ENP 504	VLSI System Design Lab	DE	0-0-2	1	
9	ENP 542	CMOS RF Design Lab	DE	0-0-2	1	
10	ENP 522	MEMS and NEMS Lab	DE	0-0-2	1	
11	ENP 546	Embedded Systems Lab	DE	0-0-2	1	

III Total credits to be earned for the completion of the degree program:

a) Through DC Category courses = 24 credits
b) Project: Phase 1 & 2 (DC) = 12 credits
c) Through DE Category courses = 17 credits

Total Credits = 53 Credits

Course content description

Course Name: ENL 509 - Advanced Device Physics

Prerequisites: Nil

Offered in: I Semester (Odd Semester)

Scheme and Credit: [(3-0-2); Credits: 4]

Type of Course: Core

Weightage: Theory-75%, Practical-25%.

Course Theory Assessment: Sessional I (20%), Sessional II (20%), Internal assessment through Assignments /Seminar /Quizzes (10%), End Semester exam (50%).

Course Objectives

1. To understand the basics of Semiconductor Physics.
2. To understand the details of Semiconductor Junctions.
3. To understand the MOS transistor details and its various models.

Course Outcomes

1. Develop skill in understanding the Semiconductor Physics
2. Ability to understand and utilize the mathematical models of semiconductor junctions and MOS transistors

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	M	M	L	L	H	H	H	-	H	L	L	L
CO2	L	L	-	M	H	M	M	L	H	L	M	M
CO3	H	M	-	H	H	H	L	L	H	L	H	H
Overall	M	M	L	M	H	H	M	L	H	L	M	M

Content (CO wise)
Introduction to Semiconductor Physics: Review of Quantum Mechanics, Electrons in periodic Lattices, E-k diagrams.

Quasi-particles in semiconductors. Boltzmann transport equation. Carrier statistics; Continuity equation, Poisson's equation and its solution; High field effects

Semiconductor junctions: Schottky, Homo- and Hetero-junction band diagrams and I-V characteristics, and small signal switching models; Two terminal and Surface states devices based on semiconductor junctions.

MOS structures: Semiconductor surfaces; The ideal and non ideal MOS capacitor band diagrams and CVs; Effects of oxide charges, defects and interface states; Characterization of MOS capacitors: HF and LF CVs, avalanche injection; High field effects and breakdown.

The MOS transistor: Pao-Sah and Brews models; Short channel effects in MOS transistors. Hot carrier effects in MOS transistors; Quasi-static compact models of MOS transistors.

Measurement of MOS transistor parameters: Scaling and transistors structures for ULSI; Silicon-on-insulator transistors; High-field and radiation effects in transistors.

Laboratory: Practicals based on theory.

Text Books

1. B. G. Streetman, and S. K. Banerjee, Solid State Electronic Devices, 7th edition, Pearson, 2014.
2. S. M. Sze and K. N. Kwok, Physics of Semiconductor Devices, 3rd edition, John Wiley & Sons, 2006.

Reference Books

1. C.T. Sah, Fundamentals of solid state electronics, World Scientific Publishing Co Inc, 1991.
2. Y. Tsividis and M. Colin, Operation and Modeling of the MOS Transistor. Oxford Univ. Press, 2011.

Course Name: ENL 511 - CMOS Digital VLSI Design

Prerequisites: Nil

Offered in: I Semester (Odd Semester)

Scheme and Credit: [(3-0-2); Credits: 4]

Type of Course: Core

Weightage: Theory-75%, Practical-25% .

Course Theory Assessment: Sessional I (15%), Sessional II (15%), Internal assessment through Assignments /Seminar /Quizzes (10%), End Semester exam (60%).

Course Objectives

1. To design and optimize CMOS Digital Integrated Circuits.
2. To understand floor planning and layout issues for digital circuits.

Course Outcomes

1. Ability to design different CMOS circuits using various logic families along with circuit layout.
2. Ability to use tools for VLSI IC design.

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	H	H	H	H	H	H	L	M	M	L	L	L
CO2	H	H	H	H	H	-	L	L	-	L	M	M
Overall	H	H	H	H	H	H	L	L	M	L	L	L

Content (CO wise)

Review of MOS transistor models, Non-ideal behavior of the MOS Transistor.

Transistor as a switch. Inverter characteristics. Integrated Circuit Layout: Design Rules, Parasitics.

Delay: RC Delay model, linear delay model, logical path efforts.

Power, interconnect and Robustness in CMOS circuit layout

Combinational Circuit Design: CMOS logic families including static, dynamic and dual rail logic.

Sequential Circuit Design: Static circuits. Design of latches and Flip-flops.

Laboratory: Practical Based on SPICE simulation of the above Syllabus. Circuit Simulation: SPICE, Device characterization, Circuit Characterization.

Text Books

1. N.H.E. Weste and D.M. Harris, CMOS VLSI design: A Circuits and Systems Perspective, 4th Edition, Pearson Education India, 2011.
2. L. Glaser and D. Dobberpuhl, The Design and Analysis of VLSI Circuits, Addison Wesley,1985.

Reference Books

1. C. Mead and L. Conway, Introduction to VLSI Systems, Addison Wesley,1979.
2. J. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice Hall India, 1997.
3. P. Douglas, VHDL: programming by example, McGraw Hill, 2013 .

Course Name: ENL 513 - IC Design with HDL

Prerequisites: Nil

Offered in: I Semester (Odd Semester)

Scheme and Credit: [(3-0-2); Credits: 4]

Type of Course: Core

Weightage: Theory-75%, Practical-25%

Course Theory Assessment: Sessional I (15%), Sessional II (15%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (60%).

Course Objectives

1. To model digital circuit using HDL and test its functionality.
2. To appreciate application of HDL for Circuit Synthesis and FPGA implementation.

Course Outcomes

1. Fluency in using hardware description languages with various design styles.
2. Ability to implement Digital IC designs.

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	H	H	H	H	H	H	L	L	L	L	L	L
CO2	L	L	H	L	H	M	-	-	L	L	M	-
Overall	H	H	H	M	H	M	L	L	L	L	L	L

Content (CO wise)
Basic concepts of hardware description languages.

Hierarchy, Concurrency, Logic and Delay modeling.

Structural, Data-flow and Behavioral styles of hardware description. Architecture of event driven simulators.

Syntax and Semantics of HDL: Variable and signal types, arrays and attributes. Operators, expressions and signal assignments. Entities, architecture specification and configurations. Component instantiation.

Concurrent and sequential constructs. Use of Procedures and functions,

Examples of design using VHDL or Verilog. Synthesis of logic from hardware description.

Laboratory: Practicals based on the above theory and FPGA implementation

Text Books

1. Z. Navabi, VHDL, International Edition, McGraw Hill, 1998.
2. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall NJ, USA,1996.

Reference Books

1. J. Bhaskar, VHDL Primer, Pearson Education Asia, 2001.
2. J. Bhaskar, Verilog HDL Synthesis - A Practical Primer, Star Galaxy Publishing, Allentown, PA,1998.

Course Name: ENL 517 - Micro and Nano Fabrication Technologies

Prerequisites: Nil

Offered in: I Semester (Odd Semester)

Scheme and Credit: [(3-0-2); Credits: 4]

Type of Course: Core

Weightage: Theory-75%, Practical-25%

Course Theory Assessment: Sessional I (20%), Sessional II (20%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (50%).

Course Objectives

1. To get exposed tocurrent state of the art Micro and Nano Fabrication Technologies in Semiconductor Industry
2. To understand manufacturing methods and their underlying scientific principles in the context of technologies used in VLSI/ULSI chip fabrication

Course Outcomes

1. Ability to appreciate the various VLSI/ULSI fabrication technologies.
2. To design the process of VLSI circuit fabrication.

Mapping with POs (Departmental reference) :

Relationship of Course Objectives to Program outcomes:

The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	M	M	L	-	M	H	H	L	L	-	-	H
CO2	H	H	-	L	M	L	H	-	-	L	L	M
Overall	M	M	L	L	M	L	H	L	L	L	L	M

Content (CO wise)

General overview of current status of Micro and Nano fabrication technologies: Interaction between Technology and Design, Interaction between Physics and Technology,Limits of Technology.

Environment for Integrated Circuits Manufacture: Clean Rooms and Wafer cleaning procedures, Technology details of the Laboratory, Contamination Control.

Processes in Fabrication: Deposition (PVD: Sputtering, Evaporation, MBE, PLD(epitaxy); CVD:PECVD, LCVD, ALD),Etching (Wet, Dry, Powder Blast), Doping (Diffusion, Ion Implantation), Oxidation, Characterization of Processes.

Lithography and Mask generation techniques: Optical, Laser, X-ray, Direct(E-beam), Nanoimprint, Soft, Pattern transfer, LIGA.

Nanofabrication by Self assembly: Self Assembly Process (top-down and bottom-up),Nanosystem and Building Blocks; Enabling Technologies: Wafer Planarization(CMP) and Bonding.

Device Fabrication examples: NMOS Technology, Mask sequence based fabrication process for NMOS transistors, Silicon Gate and Metal Gate Technologies, Limitations of NMOS Technology.

Laboratory: Practicals based on the theory

Text books

1. S. A. Campbell, Fabrication Engineering at the Micro- and Nanoscale, 4th edition, Oxford University Press, 2008.
2. J.D. Plummer, Silicon VLSI technology: Fundamentals, Practice and Modeling, Pearson Education India, 2009.

References

1. H. H. Gatzen and S. Volker, Micro and Nano Fabrication-Tools and Processes, Springer, 2015.
2. C.Y. Chang, S.M. Sze, ULSI Technology , McGraw-Hill, 1996.
3. Richard C.Jaeger, Introduction to Microelectronic Fabrication: Volume 5 of Modular Series on Solid State Devices, Pearson, 2002.
4. S. K. Ghandhi, VLSI Fabrication Principles: Silicon and Gallium Arsendie, 2nd Edition, John Wiley and Sons, 1994.

Course Name: ENL 518 - Analog IC Design

Prerequisites: Nil

Offered in: II Semester (Even Semester)

Scheme and Credit: [(3-0-2); Credits:4]

Type of Course: Core

Weightage: Theory-75%, Practical-25%

Course Theory Assessment: Sessional I (15%), Sessional II (15%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (60%).

Course Objectives

1. To study Basics of analog IC designing.
2. To understand the Frequency response, stability and noise issues in Analog Circuits.
3. To understand the implementation of linear and non – linear analog block implementation and their testing.

Course Outcomes

1. Developed ability to design analog building blocks of VLSI circuit.
2. Developed ability to build SPICE deck of MOS integrated circuits.

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	H	H	H	H	H	M	L	-	L	-	M	M
CO2	H	M	M	H	H	L	-	L	-	L	M	M
CO3	L	L	L	H	H	-	L	-	-	L	-	-
Overall	M	M	M	H	H	L	L	L	L	L	M	M

Content (CO wise)
Overview of noise in analog circuits. Basic analog MOS models, SPICE Models and frequency dependent parameters.

Current Mirrors: Current matching, temperature behavior, cascade current mirror. Wide swing current mirror. Short channel Current Mirror design. Voltage references.

Single Stage Amplifier: Common Source amplifiers, Source follower, Current Source loads, Cascode Amplifier, level shifter. Output stage Class AB and Push-Pull amplifier. Frequency response and stability considerations.

Differential Amplifier: Source coupled pair. Source cross-coulpled pair. Cascode loads. Wide swing differential amplifiers.

Operational Amplifiers: Two stage OA. Output buffer. OTA. Gain Enhancement. Biasing for Power and speed. CMFB.

Data Converter fundamentals. DAC, ADC specifications.. R-2R ladder, charge scaling, cyclic and pipelined DACs. Flash, pipeline, SAR, Integrating and Sigma Delta ADCs

Laboratory: Practicals based on the theory

Text Books

1. R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, 4th edition Wiley, 2005.
2. M. Ismail, Analog VLSI: Signal and Information Process, McGraw-Hill ,1994.

Reference Books

1. P.R. Gray and R.G. Meyer, Analysis and design of Analog Integrated circuits, 3rd Edition, John Wiley and Sons, 1993.
2. B. Razavi, Design of Analog CMOS Integrated Circuits, Prentice-Hall,1998.

Course Name: ENL 520 - Nanoelectronics

Prerequisites: Nil

Offered in: II Semester (Even Semester)

Scheme and Credit: [(3-0-2); Credits: 4]

Type of Course: Core

Weightage: Theory-75%, Practical-25%

Course Theory Assessment: Sessional I (15%), Sessional II (15%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (60%).

Course Objectives

1. To get introduced to Nanoelectronics and nanotechnology.
2. To understand working of Nano scale transistor.
3. To understand modeling aspects of Nanoscale devices from perspective of circuit applications.

Course Outcomes

1. Building molecular level devices and systems.
2. Design of Carbon based Nanoelectronic devices

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	-	-	L	M	L	-	H	-	M	M	H	L
CO2	L	L	-	L	L	-	-	-	-	-	M	M
CO3	L	L	L	L	L	L	L	M	-	L	-	-
Overall	L	L	L	L	L	L	M	M	M	L	M	M

Content (CO wise)
Basics of Quantum Mechanics: Schrodinger equation, Density of States. Particle in a box Concepts, Degeneracy.

Band Theory of Solids. Kronig-Penny Model. Brillouin Zones.

Shrink-down approaches: Introduction, CMOS Scaling, The nanoscale MOSFET, Finfets, Vertical MOSFETs, limits to scaling, system integration limits (interconnect issues etc.),

Resonant Tunneling Diode, Single electron transistors,

Carbon nanotube electronics, Bandstructure and transport, devices, applications

2D semiconductors, Graphene, transition metal dichalcogenides, atomistic simulations

Laboratory: Practicals based on the theory

Text Books

1. G.W. Hanson, Fundamentals of Nanoelectronics, Pearson, 2009.
2. W. Ranier, Nanoelectronics and Information Technology (Advanced Electronic Materials and Novel Devices), Wiley-VCH, 2003.

Reference Books

1. K.E. Drexler, Nanosystems, Wiley, 1992.
2. J.H. Davies, The Physics of Low-Dimensional Semiconductors, Cambridge University Press, 1998.
3. C. P. Poole, F. J. Owens, Introduction to Nanotechnology, Wiley, 2003.

Course Name: ENL504 - VLSI System Design

Prerequisites: Nil

Offered in: II Semester (Even Semester)

Scheme and Credit: [(3-0-0); Credits: 3]

Type of Course: Elective

Course Theory Assessment: Sessional I (15%), Sessional II (15%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (60%).

Course Objectives

1. To use hierarchical methodologies for system hardware design.
2. To understand the use of finite state machines in VLSI system design.
3. To understand various design issues in the VLSI system implementation.

Course Outcomes

1. To acquire skills for VLSI system design
2. Implementation understanding for chip layout

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	H	H	L	H	H	H	H	M	H	L	L	L
CO2	L	L	-	H	H	-	-	-	-	L	M	M
CO3	L	M	L	H	H	-	L	M	-	L	-	M
Overall	M	M	L	H	H	H	M	M	H	L	M	M

Content (CO wise)
Introduction to System Design, Challenges in VLSI System Design, Scaling trends and their effects on system design.

Interconnect issues, Signal Interconnect Models: Lumped, Distributed, Delay and Cross-talk, Buffer Design, Power and Clock Distribution.

Design of Finite State Machines, State Assignment Strategies, State Machine Reuse.

RTL Design, ASM Chart, Decomposition of System into Data Path and Control Path.

Parallelism and System Decomposition, Pipelining, Use of Data Flow Graphs, Critical Path Analysis and Parallel Processing.

Introduction to Queuing theory applied to the Digital System Architecture. Layout strategies at IC and board level for local and global signals. Memory Sub-System Design

Text Books

1. W. Wolf, Modern VLSI Design: System-on-chip Design, 3rd Edition, Pearson, 2002.

Reference Books

1. R. Seetharaman, Digital VLSI System Design, Springer, 2007.
2. J. M. Rabaey, Digital Integrated Circuits, Prentice Hall of India, 1997.

Course Name: ENP 504 - VLSI System Design Lab

Offered in: II Semester (Even Semester)

Scheme and Credit: [(0-0-2); Credits: 1]

Type of Course: Elective

Content (CO wise)

Laboratory based on the Theory Course and involves design and simulation using EDA tools

Course Name: ENL 542 - CMOS RF Design

Prerequisites: Nil

Offered in: II Semester (Even Semester)

Scheme and Credit: [(3-0-0); Credits: 3]

Type of Course: Elective

Course Theory Assessment: Sessional I (20%), Sessional II (20%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (50%).

Course Objectives

1. To understand the necessity and the issues involved in design of CMOS Circuits for GHz Frequencies using active and passive components
2. To understand PCB design at GHz frequencies

Course Outcomes

1. Ability to design and test CMOS RF Circuit and systems
2. Development of skills for designing and testing of PCBs at GHz frequencies

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	L	M	L	M	H	H	H	M	H	L	L	L
CO2	L	L	-	M	H	-	L	-	-	L	M	-
Overall	L	M	L	M	H	H	M	M	H	L	M	L

Content (CO wise)
Introduction to High Speed Circuit Design; Transmission line theory

Noise Analysis: Sources, Noise Figure, Gain compression, Harmonic distortion, Intermodulation, Cross-modulation, Dynamic range

Devices: Passive and active, Lumped passive devices(models), Active(models,low vs high frequency)

Amplifier Design: Low Noise Amplifiers Power Amplifiers; Mixers: Up Conversion & Down Conversion

Oscillators: Principles, Phase Noise; PLL; Transceiver architectures

PCB Design: Anatomy, Board Assembly, Thermal Management

Laboratory Course: Laboratory based on the above contents involves design and simulation using CAD tools. Design of Passives, Interconnects and Characterization of PCB Signal lines.

Text books

1. T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, 2004.
2. B. Razavi, RF Microelectronics, 2nd Edition, Prentice-Hall, 2012.

Reference books

1. G. Gonzalez, Microwave Transistor Amplifiers, 2nd Edition, Prentice Hall, 1997.
2. D. Pozar, Microwave Engineering, 4th Edition, Wiley, 2011.
3. K. Chang, RF and Microwave Wireless systems, Wiley, 2002.

Course Name: ENP 542 - CMOS RF Design Lab

Offered in: II Semester (Even Semester)

Scheme and Credit: [(0-0-2); Credits: 1]

Type of Course: Elective

Content (CO wise)

Laboratory based on the Theory Course and involves design and simulation using EDA tools

Course Name: ENL 522 - MEMS and NEMS

Prerequisites: Nil

Offered in: II Semester (Even Semester)

Scheme and Credit: [(3-0-0); Credits: 3]

Type of Course: Elective

Course Assessment Method: Sessional I (15%), Sessional II (15%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (60%).

Course Objectives

1. To understand the multidisciplinary aspects of MEMS and NEMS devices and their applications
2. To understand their fabrication and modeling methods.

Course Outcomes

1. Appreciate the underlying working principles of MEMS and NEMS devices
2. Ability to design and model these devices

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	-	L	L	-	H	H	H	M	H	L	L	L
CO2	L	L	-	M	H	H	-	-	-	L	M	M
Overall	L	M	L	M	H	H	H	M	H	L	L	L

Content (CO wise)
Introduction and Historical Background, Scaling Effects. Micro/Nano Sensors, Actuators and Systems overview: Case studies.

Review of Basic MEMS/NEMS fabrication modules: Oxidation, Deposition Techniques, Lithography(LIGA), Etching.

Micromachining: Surface Micromachining, sacrificial layer processes, Stiction; Bulk

Micromachining, Isotropic Etching and Anisotropic Etching, Wafer Bonding.

Mechanics of solids in MEMS/NEMS: Stresses, Strain, Hookes's law, Poisson effect, Linear Thermal Expansion, Bending; Energy methods.

Brief Overview of Finite Element Method. Modeling of Coupled Electromechanical Systems.

Laboratory Course: Laboratory based on the above contents involves design and simulation using CAD tools

Text Book

1. G. K. Ananthasuresh, K. J. Vinoy, S. Gopalkrishnan, K. N. Bhat, V. K. Aatre, Micro and Smart Systems, Wiley India, 2012.
2. S. E.Lyshevski, Nano-and Micro-Electromechanical systems: Fundamentals of Nano-and Microengineering (Vol. 8). CRC press, (2005).

Reference Books

1. S. D. Senturia, Microsystem Design, Kluwer Academic Publishers, 2001.
2. M. Madou, Fundamentals of Microfabrication, CRC Press, 1997.
3. G. Kovacs, Micromachined Transducers Sourcebook, McGraw-Hill, Boston, 1998.
4. M.H. Bao, Micromechanical Transducers: Pressure sensors, accelerometers, and gyroscopes, Elsevier, New York, 2000.
5. Journals: 1. Journal of Micrelectromechanical Systems, IEEE/ASME. 2. IEEE Transactions on Nanotechnology.

Course Name: ENP 522 - MEMS and NEMSLab

Offered in: II Semester (Even Semester)

Scheme and Credit: [(0-0-2); Credits: 1]

Type of Course: Elective

Content (CO wise)

Laboratory based on the Theory Course and involves design and simulation using EDA tools

Course Name: ENL 546 - Embedded Systems

Prerequisites: Nil

Offered in: II Semester (Even Semester)

Scheme and Credit: [(3-0-0); Credits: 3]

Type of Course: Elective

Course Theory Assessment: Sessional I (15%), Sessional II (15%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (60%).

Course Objectives

1. To understand advanced concepts of Embedded System Architecture
2. To design systems for various embedded control applications.

Course Outcomes

1. Ability to design high-speed system using embedded cores
2. Analysis of Hardware Software co-design trade-offs

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	L	L	L	-	H	H	H	M	H	L	L	L
CO2	L	L	-	M	H	H	-	-	-	L	-	-
Overall	L	L	L	M	H	H	H	M	H	L	L	L

Content (CO wise)
Embedded Computing: Overview, Design Process,

System Architecture: CISC and RISC instruction set architecture, embedded Processor/Microcontroller Architecture, DSP Processors, Harvard Architecture,

Memory System Architecture: Types, Design, Cache Design and controllers, Virtual memory.

I/O Sub-system: Interfacing standards, Memory mapped I/O, DMA

Co-processors and Hardware Accelerators, Processor Performance Enhancement, CPU Power Consumption.

On Chip Buses and Interconnects

Laboratory: Programming Embedded Systems: Program Design, Programming Languages, Desired Language Characteristics, High Level Languages, Basic Compilation Techniques. Embedded System Development: Design Methodologies, UML as Design tool, Hardware-Software Partitioning/Integration.

Text books

1. V. C. Hamacher, Z. G. Vranesic, S. G. Zaky, Computer Organization, McGraw-Hill, 2002.
2. J..L.Hennesy and D.A.Patterson, Computer Architecture: A Quantitative approach, Morgan Kaufmann, 2006.

Reference books

1. M. Bass, Programming Embedded Systems in C and C++, O'Reilly Media, 1999.
2. F. Vahid and T. Gwargie, Embedded System Design, John Wiley and Sons, 1999.
3. D. E.Simon, An Embedded Software Primer, Perason Education, 2002.

Course Name: ENP 546 - Embedded Systems Lab

Offered in: II Semester (Even Semester)

Scheme and Credit: [(0-0-2); Credits: 1]

Type of Course: Elective

Content (CO wise)

Laboratory based on the Theory Course and involves design and simulation using EDA tools

Course Name: ENL 507 - Design for Testability Yield and Reliability

Prerequisites: Nil

Offered in: III Semester (Odd Semester)

Scheme and Credit: [(3-0-0); Credits: 3]

Type of Course: Elective

Course Theory Assessment: Sessional I (15%), Sessional II (15%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (60%).

Course Objectives

1. To study techniques in testing of VLSI chips.
2. To understand fault models and their use in testing of VLSI Circuits.

Course Outcomes

1. Ability to use Fault models for testing various VLSI circuits.
2. Design Circuits for Testability.

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	H	H	H	M	H	H	M	L	H	L	L	M
CO2	L	H	H	M	H	-	M	L	H	-	-	M
Overall	M	H	H	M	H	H	M	L	H	L	L	M

Content (CO wise)
Scope of testing and verification in VLSI design process. Issues in test and verification of complex chips, embedded cores and SOCs.

Fundamentals of VLSI testing. Fault models. Automatic test pattern generation. Design for testability. Scan design. Test interface and boundary scan. System testing and test for SOCs. Iddq testing. Delay fault testing.

BIST for testing of logic and memories. Test automation.

Design verification techniques based on simulation, analytical and formal approaches.

Functional verification. Timing verification. Formal verification. Basics of equivalence checking and model checking.

Hardware emulation. Parametric testing, Reliability modeling, Yield models.

Text Books

1. M. Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Kluwer Academic Publishers,2000.

2. M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, IEEE Press, 1990.

Reference Books

1. T. Krop, Introduction to Formal Hardware Verification, Springer Verlag, 2000.

2. P. Rashinkar, L. Singh, System-on-a-Chip Verification-Methodology and Techniques, Kluwer Academic Publishers, 2001.

Course Name: ENL 521 - Real Time Signal Processing

Prerequisites: Nil

Offered in: III Semester (Odd Semester)

Scheme and Credit: [(3-0-0); Credits: 3]

Type of Course: Elective

Course Assessment Method: Sessional I (15%), Sessional II (15%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (60%).

Course Objectives

1. To understand Real Time implementation of DSP Systems
2. Exposure to DSP Application deployment

Course Outcomes

1. Real time implementation of algorithms on digital signal processors.
2. Ability to design algorithms for different DSP applications.

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	-	-	-	-	M	M	H	M	H	L	L	L
CO2	-	L	-	L	L	L	H	M	H	L	-	L
Overall	-	L	-	L	M	L	H	M	H	L	L	L

Content (CO wise)
Basic Elements of Real Time DSP Systems, Analog Interface for Real Time DSP systems, Oversampling ADC, Oversampling DAC, Constraint of Real Time Signal Processing

Digital Signals and Systems, DSP System Design, Sine Wave Generators, Noise Generators, Fixed-Point Representations and Quantization Effects, Overflow and Solutions

Design of FIR and IIR Filters, Realization and Implementation Considerations of FIR and IIR filters, Practical Application of FIR and IIR filters, Interpolation and Decimation Filters

Frequency Domain Analysis, Discrete Fourier Transform, Fast Fourier Transforms, Practical Applications of Transforms, DTMF Generation and Detection

Adaptive Filters, Performance Analysis of Adaptive Filters, Practical Applications of Adaptive Filers, Adaptive Acoustic Echo Cancellation

Computer Architectures for Signal Processing, Harvard Architecture, Fixed point and Floating Point DSP Processors, Implementation of Algorithms on DSP Processors, Evaluation Boards for Real Time Signal Processing

Text Books

1. E.C. Ifeachor, B.W. Jervis, Digital Signal Processing- A Practical Approach, Second Edition, Pearson, 2002.

2. S.M. Kuo, B.H. Lee, W. Tian, Real-Time Digital Signal Processing: Fundamentals, Implementations and Applications, 3rd Edition, Wiley, 2013.

Reference Books

1. D. Stranneby, W. Walker, Digital signal processing & applications, Second Edition, Elsevier, 2004.

2. K. Sayood, Introduction to Data Compression, Second Edition, Elsevier, 2012.

3. A.M. Rao and A.S. Bopardikar, Wavelet Transforms: Introduction to Theory and Applications, Pearson Edition, 1998.

4. S. Mallat, Wavelet tour of signal processing, the sparse way, Elsevier, 2009.

Course Name: ENL 547 - Spintronics

Prerequisites: Nil

Offered in: III Semester (Odd Semester)

Scheme and Credit: [(3-0-0); Credits: 3]

Type of Course: Elective

Course Assessment Method: Sessional I (15%), Sessional II (15%), Internal assessment through assignments /Seminar /Quizzes (10%), End Semester exam (60%).

Course Objectives

1. To understand fundamentals of spin electronics, spin relaxation, spin transport in metal and semiconductors.
2. To understand advances in spin electronic technology and futuristic materials with high spin polarization.

Course Outcome

1. Ability to understand physics and technology of Spintronics
2. Learn practical knowledge of Spin dependent transport.

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	-	-	-	-	H	-	M	M	L	L	L	M
CO2	L	L	-	M	H	-	M	H	L	M	H	M
Overall	L	L	-	M	H	-	M	L	L	L	H	M

Content (CO wise)
History and overview of spin electronics, magnetic materials, Quantum Mechanics of spin, Bloch sphere.

Spin-orbit interaction, Exchange interaction, Spin relaxation mechanisms, spin relaxation in a quantum dots, spin Galvanic effect, spin-dependent transport, Spin dependent tunnelling, ferromagnet and Superconductor interfaces, Spin transfer torques.

Spin-transfer drive magnetic dynamics, domain wall scattering and Current-Induced switching in ferromagnetic wires, Spin injection, spin accumulation, and spin current, Spin hall effect.

Silicon based spin electronic devices, Spin LEDs: Fundamental and applications, Spin photoelectronic devices based on Heusler alloy, Electron spin filtering.

Materials for spin electronics, Nanostructures for spin electronics, Deposition techniques, micro and nanofabrication techniques.

Spin-Valve and spin-tunneling devices: Read Heads, MRAMS, Field Sensors, Spintronic Biosensors, Spin transistors, Quantum Computing with spins.

Text books

1. S. Bandyopadhyay, M. Cahay, Introduction to Spintronics, CRC Press, 2013.
2. M. Johnson, Magnetoelectronics, Academic Press, Elsevier, 2004.

Reference Books

1. D. J. Sellmyer, R. Skomski, Advanced Magnetic Nanostructures, Springer, 2006.
2. S. Maekawa, Concepts in Spin Electronics, Oxford University Press, 2006.
3. D.D. Awschalom, R.A. Buhrman, J.M. Daughton, S.V. Molnar, and M.L. Roukes, Spin Electronics, Kluwer Academic Publishers, 2004.
4. Y. B. Xu and S.M. Thompson, Spintronic Materials and Technology, Taylor & Francis, 2007.

Course Name: ENL 523- Display Materials and Technologies

Prerequisites: Nil

Offered in: III Semester (Odd Semester)

Scheme and Credit: [(3-0-0); Credits: 3]

Type of Course: Elective

Course Assessment Method: Sessional I (20%), Sessional II (20%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (50%).

Course Objectives

1. To provide the fundamental knowledge for understanding concepts of different display technologies related to manufacturing techniques and materials selection

Course Outcome

1. Ability to design displays
2. Learn practical knowledge of display technologies

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → COs ↓	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**	**l**
CO1	-	-	-	H	H	M	H	M	L	L	L	L
Overall	-	-	-	H	H	M	H	M	L	L	L	L

Content (CO wise)
Overview of display industry, information capacity of displays, introduction to different flat panel display technologies.

Fundamentals of Photometry, including luminance and brightness, Colorimetry: visual basis of colorimetry, psychophysical experiments to quantify color, CIE colorimetry

Characterization and performance of displays: Concepts of aspect ratio, color gamut, contrast and gradation, directional visibility, driving power, efficiency, speed, memory and storage, degradation, resolution, addressability, physiological factors, and measurement instrumentation;

Luminescence and luminescent materials: Physical processes and interactions leading to emission of light, processes responsible for the transfer of energy in luminescent materials, chemistry and preparation of luminescent materials, and emission properties of the prepared materials;

Basics of matrix addressing of displays: active and passive matrix.

Technical discussion of display technologies: LEDs, OLEDs, LCDs, Active matrix TFT back planes for OLED and LCD displays. Other displays and associated technologies.

Text books

1. W. Mara, Liquid crystal flat panel displays: manufacturing science & technology. Springer Science & Business Media, 2012.

Reference Books

1. R. H. Chen, Liquid crystal displays: fundamental physics and technology. John Wiley and Sons, 2011.

Course Name: ENL 543 - Nanophotonics

Prerequisites: Nil

Offered in: III Semester (Odd Semester)

Scheme and Credit: [(3-0-0); Credits: 3]

Type of Course: Elective

Course Assessment Method: Sessional I (20%), Sessional II (20%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (50%).

Course Objectives

1. To understand the necessity and significance of Nanophotonics
2. To understand the implementation of Nanophotonics circuits

Course Outcome

1. To appreciate Nanophotonics implemented on-chip at nanoscale
2. To design and realize Nanophotonics circuits.

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	-	-	H	H	H	H	H	M	H	L	M	L
CO2	L	L	-	M	H	-	-	-	-	L	M	M
Overall	L	L	H	M	H	H	H	M	H	L	M	L

Content (CO wise)
Introduction to Nanophotonics.

Quantum Electrodynamics: Maxwell's Equations in 1-D and 2-D structures,

Propagation of light in quantum confined structures; Quantum mechanical model of carrier distribution; Light -Matter interactions at microscopic levels.

Materials: Crystal Structure, Optoelectronic properties, Selection of materials and epitaxial growth, Common material systems such as InP-InGaAsP and GaAs-AlGaAs.

Computational Methods: Techniques like BPM, FEM, FDTD for modeling light propagation in quantum well, wire and dot structures. Semiconductor

Optical Amplifiers: Operation Principle, Application and Functionalities, Realization of Logic gates, SOA based circuits

Text books

1. J. W. Haus, Fundamentals and Applications of Nanophotonics , Woodhead Publishing, 2016.
2. S. V. Gaponenko , Introduction to Nanophotonics , Cambridge Press, 2009.

Reference Books

1. P. N. Prasad, Elements of Nanophotonics, Wiley Publication, 2004.
2. R. Ali, H. Baghban, and R. Maram, Nanostructure Semiconductor Optical Amplifiers: Building Blocks for All-optical Processing, Springer Science & Business Media,2000.

Course Name: ENL 545 - VLSI Signal Processing

Prerequisites: Nil

Offered in: III Semester (Odd Semester)

Scheme and Credit: [(3-0-0); Credits: 3]

Type of Course: Elective

Course Assessment Method: Sessional I (15%), Sessional II (15%), Internal assessment through assignments /seminar /quizzes (10%), End Semester exam (60%).

Course Objectives

1. To understand advanced concepts in signal processing elements for 1D and 2D signals.
2. To study architecture for VLSI implementation of DSP algorithms.

Course Outcomes

1. Designing of DSP system for VLSI implementation.
2. Analysis of the DSP system performance.

Mapping with POs (Departmental reference) :
Relationship of Course Objectives to Program outcomes:
The correlation of the COs with the POs are given in the following table. Letters 'H', 'M', or 'L' in a cell indicates 'high', 'medium' or 'low' correlation of the CO with the corresponding PO. A blank cell indicates no correlation.

POs → / COs ↓	a	b	c	d	e	f	g	h	i	j	k	l
CO1	L	L	L	M	H	H	H	M	H	L	L	H
CO2	L	L	-	M	H	-	H	L	-	M	M	M
Overall	L	L	L	M	H	H	H	M	H	L	L	H

Content (CO wise)
Introduction to Digital Signal Processing Systems. Iteration Bound. Pipelining and Parallel Processing.

Retiming. Unfolding. Folding. Systolic Architecture Design.

Fast Convolution: Cook- Toom Algorithm, Cyclic Convolution, Iterated Convolution

Algorithmic Strength Reduction in Filters and Transforms. Parallel FIR Filters

Pipelined and Parallel Recursive and Adaptive Filters.

Scaling and Roundoff Noise. Concepts in Synchronous, Wave, and Asynchronous Pipelines. Low Power Design.

Text Books

1. K. K. Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, John Wiley and Sons, 2007.

Reference Books

1. W. Roger, M. John, Y. Yi, G. Lightbody, FPGA-based implementation of signal processing systems, John Wiley and Sons, 2008.
2. A. V. Oppenheim, R.W. Schaefer, Discrete time Signal Processing, Prentice-Hall of India, 1989.
3. J. G. Proakies, D. G. Monolakis, Digital signal Processing: Principles, Algorithms and application, Third Edition, Prentice-Hall of India, 1996.
4. A. K. Jain, Fundamentals of Digital Image Processing, Prentice-Hall of India, 1989.
5. R. C. Gonzalez, R. E. Woods, Digital Image Processing, Second Edition, Pearson Education, 2002.